ABSTRACT

A processor is arranged to make it possible to specify an instruction for which value prediction is thought to enhance program execution performance and execute the instruction and enhance the accuracy of prediction when carrying out value prediction. The processor is provided with an instruction cache to store instructions to which a value prediction field and a value prediction method field are attached. Prior to or in concurrence with fetching and executing an instruction by its execution unit, the execution result value predicted by a value predictor designated by the contents of the value prediction method field of the instruction is output. Only when the value prediction field contains '1,' the predicted value is stored into the register and used in executing a subsequent instruction. The predicted value for an instruction with its value prediction field containing '0' is nullified. For each instruction, the result of prediction made by the value predictor is compared with the result of executing the instruction by the execution unit. When the comparison is a mismatch, the result of prediction stored in the register is cleared and the data contents of the value prediction field or value prediction method field of the instruction in the cache memory are updated.